

Amendment to the Specification:

On page 1, please add the following paragraph beginning line 6:

This application claims the benefit of priority to German patent application no. DE 10217565.9, filed April 19, 2002.

On page 1, please replace the paragraph beginning on line 6 with the following amended paragraph:

TECHNICAL FIELD

The present invention relates to a semiconductor component having a semiconductor substrate on which an insulating layer is produced, the insulating layer having a capacitance structure produced in it.

On page 1, please replace the paragraph beginning on line 11 with the following amended paragraph:

BACKGROUND

Most analog circuit parts of hybrid digital/analog circuits require capacitors having a high capacitance value, a high level of linearity and high quality. In order to keep the costs for fabricating the component as low as possible, it is necessary for the fabrication of the capacitance structures to require as few process steps as possible. In addition, the progressive miniaturization of the components and integrated circuits also entails the demand for as little area requirement as possible for the capacitance structure.

On page 3, please replace the paragraph beginning on line 3 with the following amended paragraph:

BRIEF SUMMARY

It is therefore an object of the present invention to provide a semiconductor component having an integrated capacitance structure where the ratio of useful capacitance to parasitic capacitance can be improved.

On page 7, please replace the paragraph beginning on line 4 with the following amended paragraph:

BRIEF DESCRIPTION OF THE DRAWING

A plurality of exemplary embodiments of the inventive semiconductor component are explained in more detail below with reference to schematic drawings, in which:

On page 7, please replace the paragraph beginning on line 30 with the following amended paragraph:

DETAILED DESCRIPTION

A semiconductor component based on the invention (Figure 1) has a capacitance structure K which is produced in an insulating layer or insulating layer system (not shown). The insulating layer and the capacitance structure K are arranged on a semiconductor substrate (not shown). In the exemplary embodiment, the capacitance structure K has a first substructure T1a. The substructure T1a is produced from a metal latticed region G1a and a plurality of metal plates P1a. Each of the cutouts in the latticed region G1a has a metal plate F1a centrally arranged in it. The metal plates F1a and the latticed region G1a are produced in one metallization plane M1, the latticed region G1a being electrically connected to a first connecting line (not shown) and forming an electrode for the

capacitance structure K. The metal plates F1a are electrically connected to a second connecting line (not shown). This forms first useful capacitance components of the capacitance structure in the metallization plane M1. These capacitance components C, (shown in Figure 5) are respectively formed between the surface regions of the latticed region G1a and of a metal plate F1a which are opposite one another in the metallization plane M1.